

**Amendments to the claims**

Please amend claims 1 and 10 as shown in the following listing of claims. This listing of claims will replace all prior versions, and listings, of claims in the application.

- 1 1. (currently amended) A semiconductor structure comprising:  
2 a semiconductor core having a side surface;  
3 a layer of insulating material on said side surface, said layer of  
4 insulating material covering the entire said side surface; and  
5 electrically isolated electrodes arrayed along said layer of  
6 insulating material on said side surface, said electrically isolated electrodes  
7 including a conductive material having etch selectivity with respect to said  
8 insulating material.
- 1 2. (original) The semiconductor structure of claim 1 wherein said electrically  
2 isolated electrodes extend substantially in a direction orthogonal to a major  
3 surface of said semiconductor core, said major surface being orthogonal to said  
4 side surface.
- 1 3. (original) The semiconductor structure of claim 1 wherein said conductive  
2 material includes silicon-based conductive material.
- 1 4. (original) The semiconductor structure of claim 3 wherein said silicon-  
2 based conductive material includes polysilicon.
- 1 5. (original) The semiconductor structure of claim 1 wherein said  
2 semiconductor core includes single-crystal silicon.
- 1 6. (original) The semiconductor structure of claim 1 wherein said insulating  
2 material of said layer includes oxide of said semiconductor core.

1 7. (original) The semiconductor structure of claim 1 wherein said electrically  
2 isolated electrodes are additionally arrayed over a major surface of said  
3 semiconductor core, said major surface being orthogonal to said side surface.

1 8. (original) The semiconductor structure of claim 7 further comprising  
2 interconnects electrically connected to selected ones of said electrically isolated  
3 electrodes, said interconnects being positioned over said major surface of said  
4 semiconductor core.

1 9. (original) The semiconductor structure of claim 7 wherein said electrically  
2 isolated electrodes are additionally arrayed along a second side surface of said  
3 semiconductor core.

1 10. (currently amended) A semiconductor structure comprising:  
2 a semiconductor core having a major surface and a side surface,  
3 said major surface being orthogonal to said side surface, said side surface being a  
4 planar surface;  
5 a continuous layer of insulating material on said side surface, said  
6 continuous layer of insulating material covering the entire said side surface; and  
7 electrically isolated electrodes arrayed along said continuous layer  
8 of insulating material on said side surface such that said electrically isolated  
9 electrodes extend substantially in a direction orthogonal to said major surface, said  
10 electrically isolated electrodes including conductive material having etch  
11 selectivity with respect to said insulating material.

1 11. (original) The semiconductor structure of claim 10 wherein said  
2 conductive material includes silicon-based conductive material.

1 12. (original) The semiconductor structure of claim 11 wherein silicon-based  
2 conductive material includes doped polysilicon.

1 13. (original) The semiconductor structure of claim 10 wherein said  
2 semiconductor core includes single-crystal silicon.

1 14. (original) The semiconductor structure of claim 10 wherein said  
2 electrically isolated electrodes additionally extend over said major surface of said  
3 semiconductor core.

1 15. (original) The semiconductor structure of claim 14 further comprising  
2 interconnects electrically connected to selected ones of said electrically isolated  
3 electrodes, said interconnects being positioned over said major surface of said  
4 semiconductor core.

1 16. (withdrawn) A method for fabricating a semiconductor structure, the  
2 method comprising:  
3 providing a semiconductor core with a side surface;  
4 forming a layer of insulating material on said side surface of said  
5 semiconductor core;  
6 forming a layer of conductive material adjacent to said layer of  
7 insulating material on said side surface, said conductive material having etch  
8 selectively with respect to said insulating material; and  
9 selectively etching said layer of conductive material using a stop-  
10 on-oxide deep reactive ion etching to define electrically isolated electrodes  
11 arrayed along said layer of insulating material on said side surface.

1 17. (withdrawn) The method of claim 16 wherein said selectively etching  
2 includes selectively etching said layer of conductive material using said stop-on-  
3 oxide deep reactive ion etching such that said electrical isolated electrodes extend  
4 substantially in a direction orthogonal to a major surface of said semiconductor  
5 core, said major surface being orthogonal to said side surface.

1 18. (withdrawn) The method of claim 16 wherein said forming of said layer  
2 insulating material includes forming a layer of oxide on said side surface of said  
3 semiconductor core.

1 19. (withdrawn) The method of claim 16 wherein said forming of said layer of  
2 conductive material includes forming a layer of silicon-based conductive material  
3 adjacent to said layer of insulating material.

1 20. (withdrawn) The method of claim 19 wherein said forming of said layer of  
2 silicon-based conductive material includes forming a layer of polysilicon adjacent  
3 to said layer of insulating material.

1 21. (withdrawn) The method of claim 16 wherein said providing of said  
2 semiconductor core includes providing a single-crystal silicon core with said side  
3 surface.

1 22. (withdrawn) The method of claim 16 wherein said forming of said layer of  
2 conductive material includes forming said layer of conductive material over a  
3 major surface of said semiconductor core, said major surface being orthogonal to  
4 said side surface, and wherein said selectively etching of said layer of conductive  
5 material includes selectively etching said layer of conductive material over said  
6 major surface of said semiconductor core using said stop-on-oxide deep reactive  
7 ion etching such that said electrically isolated electrodes extend over said major  
8 surface of said semiconductor core.

1 23. (withdrawn) The method of claim 22 further comprising forming  
2 interconnects over said major surface of said semiconductor core, said  
3 interconnects being electrically connected to selected ones of said electrically  
4 isolated electrodes.